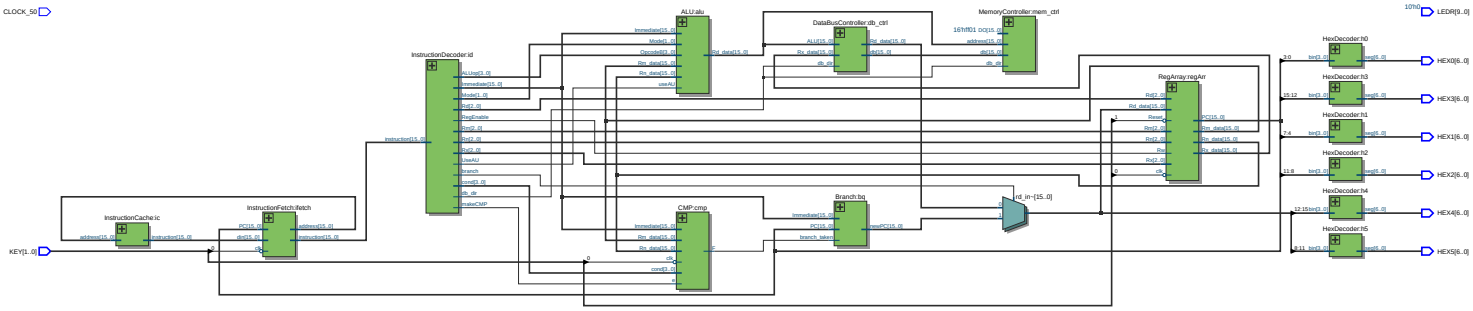
CLOCK_50
KEY[1..0]
InstructionCache:ic
address[15..0]
instruction[15..0]
InstructionFetch:fetch
PC[15..0]
din[15..0]
rd
address[15..0]
instruction[15..0]
InstructionDecoder:id
instruction[15..0]
ALUop[3..0]
Immediate[15..0]
Mode[1..0]
Opcode[31..0]
Rm_data[15..0]
Rn_data[15..0]
useAU
PropEnable
Rm[2..0]
Rn[2..0]
Rd[2..0]
UseAU
branch
cond[3..0]
rb_dir
disableCMP
ALU:alu
Immediate[15..0]
Mode[1..0]
Opcode[31..0]
Rm_data[15..0]
Rn_data[15..0]
useAU
Rd_data[15..0]
DataBusController:db_ctrl
ALU[15..0]
Rx_data[15..0]
rb_dir
Rd_data[15..0]
DB[15..0]
MemoryController:mem_ctrl
16'hff01
oc[15..0]
address[15..0]
din[15..0]
rb_dir
CMP:cmp
Immediate[15..0]
Rm_data[15..0]
Rn_data[15..0]
rb
cond[3..0]
e
f
Branch:bq
Immediate[15..0]
PC[15..0]
branch_taken
newPC[15..0]
rd_in~[15..0]
RegArray:regArr
Rd[2..0]
Rd_data[15..0]
Rwe
Rm[2..0]
Rn[2..0]
Rx
Rx[2..0]
clk
PC[15..0]
Rm_data[15..0]
Rn_data[15..0]
Rx_data[15..0]
10'h0
LEDR[9..0]
HexDecoder:h0
bin[3..0]
reg[6..0]
HEX0[6..0]
HexDecoder:h3
bin[3..0]
reg[6..0]
HEX3[6..0]
HexDecoder:h1
bin[3..0]
reg[6..0]
HEX1[6..0]
HexDecoder:h2
bin[3..0]
reg[6..0]
HEX2[6..0]
HexDecoder:h4
bin[3..0]
reg[6..0]
HEX4[6..0]
HexDecoder:h5
bin[3..0]
reg[6..0]
HEX5[6..0]